

**AMENDMENTS TO THE CLAIMS:**

Please amend the claims as follows:

1. (Currently Amended) A semiconductor device having a pixel matrix circuit that includes a pixel TFT and a storage capacitor, ~~comprising~~:

wherein the pixel TFT has a channel formation region formed above over a first wiring line through with an insulating layer interposed therebetween, and has a low concentration impurity region that is in contact with the channel formation region and overlaps the first wiring line; and

wherein the storage capacitor is formed:

from a capacitor wiring line, ~~formed on the same layer as the first wiring line,~~

from a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and

from a part of the insulating layer; and

wherein the first wiring line and the capacitor wiring line are formed on the same layer.

2. (Currently Amended) A semiconductor device having a plurality of pixels which include a pixel TFT and a storage capacitor, ~~comprising~~:

wherein the pixel TFT has a channel formation region formed above over a first wiring line with a first insulating layer and a second insulating layer interposed between the channel formation region and the first wiring line, and has a low concentration impurity region that is in contact with the channel formation region and overlaps the first wiring line; and

wherein the storage capacitor is formed:

from [[a]] the capacitor wiring line ~~formed on the same layer as the first wiring line,~~

from a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and

from the first insulating layer; and

wherein the first wiring line and the capacitor wiring line are formed on the same layer.

3. (Currently Amended) A semiconductor device having a plurality of pixels which include a pixel TFT and a storage capacitor, ~~comprising:~~

wherein the pixel TFT has a channel formation region formed ~~above~~ over a first wiring line with a first insulating layer, a second insulating layer, and a silicon oxide film interposed between the channel formation region and the first wiring line, and has a low concentration impurity region that is in contact with the channel formation region and overlaps the first wiring line; and

wherein the storage capacitor is formed:

from a capacitor wiring line ~~formed on the same layer as the first wiring line,~~

from a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and

from a laminate of the first insulating layer and the silicon oxide film; and

wherein the first wiring line and the capacitor wiring line are formed on the same layer.

4. (Previously Presented) A semiconductor device according to any one of claims 1 to 3, wherein the first wiring line is appropriately a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination, or a laminate of the conductive films, the alloy films, or the silicide films.

5. (Previously Presented) The semiconductor device according to any one of claims 1 to 3, wherein the channel formation region of the pixel TFT and the semiconductor region of the storage capacitor are formed of the same semiconductor layer.

6. (Previously Presented) A semiconductor device according to any one of claims 1 to 3, wherein the first insulating layer is appropriately an oxide or halogenated compound containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), barium (Ba), hafnium (Hf), bismuth (Bi), tungsten (W), thorium (Th), and lead (Pb).

7. (Previously Presented) A semiconductor device according to any one of claims 1 to 3, wherein the first wiring line is in floating state.

8. (Previously Presented) A semiconductor device according to any one of claims 1 to 3, wherein the first wiring line is kept at the lowest power supply electric potential.

9. (Previously Presented) A semiconductor device according to any one of claims 1 to 3, wherein the pixel TFT is connected to the source wiring line and the gate wiring line, and the storage capacitor is formed under the source wiring line and/or the gate wiring line.

10. (Currently Amended) A semiconductor device having a pixel matrix circuit and a driver circuit that are formed ~~on~~ over the same substrate, ~~comprising~~:

wherein a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit each have a channel formation region formed ~~above~~ over a first wiring line ~~through~~ with an insulating layer interposed therebetween, and each have a low concentration impurity region that is in contact with the channel formation region and overlaps the first wiring line;

wherein a storage capacitor included in the pixel matrix circuit is formed:

from a capacitor wiring line ~~formed on the same layer as the first wiring line~~,

from a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and

from a part of the insulating layer; ~~and~~

wherein the first wiring line and the capacitor wiring line are formed on the same layer; and

wherein the first wiring line connected to the pixel TFT is kept at the lowest power supply electric potential, and the first wiring line connected to the n-channel TFT is kept at the same level of electric potential as a gate electrode of the n-channel TFT.

11. (Currently Amended) A semiconductor device having a pixel matrix circuit and a driver circuit that are formed ~~on~~ over the same substrate, ~~comprising~~:

wherein a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit each have a channel formation region formed above over a first wiring line with a first insulating layer and a second insulating layer interposed between the channel formation region and the first wiring line, and each have a low concentration impurity region that is in contact with the channel formation region and overlaps the first wiring line;

wherein a storage capacitor included in the pixel matrix circuit is formed:  
from a capacitor wiring line ~~formed on the same layer as the first wiring line~~,

from a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and  
from the first insulating layer; and

wherein the first wiring line and the capacitor wiring line are formed on the same layer; and

wherein the first wiring line connected to the pixel TFT is kept at the lowest power supply electric potential, and the first wiring line connected to the n-channel TFT is kept at the same level of electric potential as a gate electrode of the n-channel TFT.

12. (Currently Amended) A semiconductor device having a pixel matrix circuit and a driver circuit that are formed on over the same substrate, comprising:

wherein a pixel TFT included in the pixel matrix circuit and an n-channel TFT included in the driver circuit each have a channel formation region formed above over a first wiring line with a first insulating layer, a second insulating layer, and a silicon oxide film interposed between the channel formation region and the first wiring, and each have a low concentration impurity region that is in contact with the channel formation region and overlaps the first wiring line;

wherein a storage capacitor included in the pixel matrix circuit is formed:  
from a capacitor wiring line ~~formed on the same layer as the first wiring line~~,

from a semiconductor region that has the same composition as the channel formation region or the low concentration impurity region, and

from a laminate of the first insulating layer and the silicon oxide film; and

wherein the first wiring line and the capacitor wiring line are formed on the same layer; and

wherein the first wiring line connected to the pixel TFT is kept at the lowest power supply electric potential, and the first wiring line connected to the n-channel TFT is kept at the same level of electric potential as a gate electrode of the n-channel TFT.

13. (Previously Presented) A semiconductor device according to any one of claims 10 to 12, wherein the first wiring line is appropriately a conductive film mainly containing an element selected from the group consisting of tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si), or an alloy film or silicide film containing the above elements in combination, or a laminate of the conductive films, the alloy films, or the silicide films.

14. (Currently Amended) The semiconductor device according to any one of claims 10 to 12, wherein the channel formation region of the pixel TFT and the semiconductor region of the storage capacitor are formed ~~of~~ on the same semiconductor layer.

15. (Previously Presented) A semiconductor device according to any one of claims 10 to 12, wherein the first insulating layer is appropriately an oxide or halogenated compound containing an element selected from the group consisting of tantalum (Ta), titanium (Ti), barium (Ba), hafnium (Hf), bismuth (Bi), tungsten (W), thorium (Th), thallium (Tl), and lead (Pb).

16. (Previously Presented) A semiconductor device according to any one of claims 10 to 12, wherein the pixel TFT is connected to the source wiring line and the gate wiring line, and the storage capacitor is formed under the source wiring line and/or the gate wiring line.

17. (Currently Amended) A semiconductor device, wherein the semiconductor device according to any one of claims ~~1 to 16~~ 1, 2, 3, 10, 11 or 12 is an active matrix liquid crystal display or an active matrix EL display.

18. (Currently Amended) A semiconductor device, wherein the semiconductor device according to any one of claims ~~1-to-16~~ 1, 2, 3, 10, 11 or 12 is a video camera, a digital camera, a projector, a projection TV, a goggle type display, an automobile navigation system, a personal computer, or a portable information terminal.

19. (New) A semiconductor device according to any one of claims 1, 2, 3, 10, 11 or 12, wherein a cross section of the first wiring is taper shaped.

20. (New) A semiconductor device according to any one of claims 1, 2, 3, 10, 11 or 12, wherein a cross section of the capacitor wiring line is taper shaped.

21. (New) A semiconductor device according to any one of claims 1, 2, 3, 10, 11 or 12, wherein a second wiring line is formed over the channel formation region with an insulating layer interposed therebetween.